Amendments to the Claims:

Please cancel claims 1, 3-8, 10, 18, 20-23 and 25 as follows. Please amend claims 2, 11, 13, 17, 19, 26, 27, 29, 33, and 43 as follows. Please add new claims 46-115 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Canceled)

2. (Currently Amended) The method of claim [[1]] 34, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

3. - 10. (Canceled)

11. (Currently Amended) The method of claim [[1]] 34, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern.

12. (Original) The method of claim 11, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

13. (Currently Amended) The method of claim [[1]] 34, wherein converting the exposed silicon pattern into a gate silicide layer and concurrently forming source/drain silicide layers, comprises

forming a metal layer on the semiconductor substrate having the exposed silicon pattern; annealing the metal layer until the exposed silicon pattern is silicided; and

removing the unreacted portion of the metal layer remaining on the spacers.

14. (Original) The method of claim 13, wherein the metal layer comprises at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

15. (Original) The method of claim 13, wherein the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti.

16. (Original) The method of claim 13, wherein the metal layer is one of a nickel layer and a nickel alloy layer.

17. (Currently Amended) The method of claim [[1]] 34, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.

18. (Canceled)

19. (Currently Amended) The method of claim [[18]]40, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

20. - 25. (Canceled)

26. (Currently Amended) The method of claim [[18]]40, further comprising forming offset spacers covering the sidewalls of the gate patterns prior to formation of the LDDs and the halos.

27. (Currently Amended) The method of claim [[18]]40, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer patterns.

28. (Original) The method of claim 27, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

29. (Currently Amended) The method of claim [[18]]40, wherein converting the exposed silicon patterns into gate silicide layers and concurrently selectively forming source/drain silicide layers, comprises:

i) forming a metal layer on the semiconductor substrate having the exposed silicon patterns;

ii) annealing the metal layer until the exposed silicon patterns are silicided; and

iii) removing the unreacted portion of the metal layer remaining on the spacers.

30. (Original) The method of claim 29, wherein the metal layer is at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

31. (Original) The method of claim 29, wherein the metal layer comprises an alloy comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

32. (Original) The method of claim 29, wherein the metal layer is a nickel layer or a nickel alloy layer.

33. (Currently Amended) The method of claim [[18]]40, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer

pattern.

34. (Previously Presented) A method of fabricating a MOS transistor comprising:

a) forming an insulated gate pattern on a semiconductor substrate, the insulated gate pattern including a silicon pattern and a sacrificial layer pattern sequentially stacked, wherein forming the insulated gate pattern comprises sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate, forming a sacrificial layer on the semiconductor substrate having the silicon layer, doping the silicon layer with impurities to control a threshold voltage prior to formation of the sacrificial layer, and sequentially patterning the sacrificial layer and the silicon layer;

b) forming spacers covering sidewalls of the gate pattern;

c) injecting impurity ions into the semiconductor substrate using the spacers and the gate pattern as ion injection masks to form source/drain regions;

d) removing the sacrificial layer pattern on the semiconductor substrate having the source/drain regions to expose the silicon pattern; and

e) converting the exposed silicon pattern into a gate silicide layer, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

35. (Previously Presented) The method of claim 34, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form a buffer layer pattern before patterning the silicon layer, and the buffer layer pattern is removed along with the sacrificial layer pattern to expose the silicon pattern.

36. (Previously Presented) The method of claim 34, wherein the impurities to control the threshold voltage are N-type.

37. (Previously Presented) The method of claim 34, wherein the impurities to control

the threshold voltage are P-type.

38. (Previously Presented) A method of fabricating a MOS transistor comprising:

a) forming an insulated gate pattern on a semiconductor substrate, the insulated gate pattern including a silicon pattern and a sacrificial layer pattern sequentially stacked;

b) forming spacers covering sidewalls of the gate pattern, impurity ions being injected into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD and a halo prior to formation of the spacers, and offset spacers being formed covering the sidewalls of the gate pattern prior to formation of the LDD and the halo;

c) injecting impurity ions into the semiconductor substrate using the spacers and the gate pattern as ion injection masks to form source/drain regions;

d) removing the sacrificial layer pattern on the semiconductor substrate having the source/drain regions to expose the silicon pattern; and

e) converting the exposed silicon pattern into a gate silicide layer, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

39. (Previously Presented) A method of fabricating a MOS transistor comprising:

a) forming an insulated gate pattern on a semiconductor substrate, the insulated gate pattern including a silicon pattern and a sacrificial layer pattern sequentially stacked;

b) forming spacers covering sidewalls of the gate pattern;

c) injecting impurity ions into the semiconductor substrate using the spacers and the gate pattern as ion injection masks to form source/drain regions;

d) removing the sacrificial layer pattern on the semiconductor substrate having the source/drain regions to expose the silicon pattern, a selective epitaxial growth layer being formed on the source/drain regions before removing the sacrificial layer pattern; and

e) converting the exposed silicon pattern into a gate silicide layer, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

40. (Previously Presented) A method of fabricating a CMOS transistor comprising:

a) defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate;

b) forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked, wherein the step of forming the insulated gate patterns comprises sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate, forming a sacrificial layer on the semiconductor substrate having the silicon layer, the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region being doped with impurities to control threshold voltages prior to formation of the sacrificial layer, and patterning the sacrificial layer and the silicon layer;

c) forming spacers covering sidewalls of the gate patterns;

d) injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain regions;

e) removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns; and

f) converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

41. (Previously Presented) The method of claim 40, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form buffer layer patterns before patterning the silicon layer, and the buffer layer patterns are removed along with the sacrificial layer patterns in order to expose the silicon patterns.

42. (Previously Presented) The method of claim 40, wherein the impurities for doping

the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region to control the threshold voltages are N-type and P-type, respectively.

43. (Currently Amended) A method of fabricating a CMOS transistor comprising:

a) defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate;

b) forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked, wherein the step of forming the insulated gate patterns comprises sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate, forming a sacrificial layer on the semiconductor substrate having the silicon layer, doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region on the semiconductor substrate having the sacrificial layer with impurities to control threshold voltages, and patterning the sacrificial layer and the silicon layer;

c) forming spacers covering sidewalls of the gate patterns;

d) injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain regions;

e) removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns; and

f) converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.
~~doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region on the semiconductor substrate having the sacrificial layer with impurities to control threshold voltages.~~

44. (Previously Presented) A method of fabricating a CMOS transistor comprising:

a) defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate;

b) forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked;

c) forming spacers covering sidewalls of the gate patterns, impurity ions being injected into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers, and offset spacers being formed covering the sidewalls of the gate patterns prior to formation of the LDDs and the halos;

d) injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain regions;

e) removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns; and

f) converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

45. (Previously Presented) A method of fabricating a CMOS transistor comprising:

a) defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate;

b) forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked;

c) forming spacers covering sidewalls of the gate patterns;

d) injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain

regions;

e) removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns, a selective epitaxial growth layer being formed on the source/drain regions before removing the sacrificial layer pattern; and

f) converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions.

46. (New) The method of claim 34, further comprising injecting impurity ions into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD and a halo prior to formation of the spacers.

47. (New) The method of claim 38, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

48. (New) The method of claim 38, wherein forming the insulated gate pattern comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

sequentially patterning the sacrificial layer and the silicon layer.

49. (New) The method of claim 48, further comprising doping the silicon layer with impurities to control a threshold voltage prior to formation of the sacrificial layer.

50. (New) The method of claim 49, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form a

buffer layer pattern before patterning the silicon layer, and the buffer layer pattern is removed along with the sacrificial layer pattern to expose the silicon pattern.

51. (New) The method of claim 49, wherein the impurities to control the threshold voltage are N-type.

52. (New) The method of claim 49, wherein the impurities to control the threshold voltage are P-type.

53. (New) The method of claim 48, further comprising doping the silicon layer on top of the semiconductor substrate with impurities to control a threshold voltage.

54. (New) The method of claim 38, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern.

55. (New) The method of claim 54, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

56. (New) The method of claim 38, wherein converting the exposed silicon pattern into a gate silicide layer and concurrently forming source/drain silicide layers, comprises

forming a metal layer on the semiconductor substrate having the exposed silicon pattern;
annealing the metal layer until the exposed silicon pattern is silicided; and
removing the unreacted portion of the metal layer remaining on the spacers.

57. (New) The method of claim 56, wherein the metal layer comprises at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

58. (New) The method of claim 56, wherein the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti.

59. (New) The method of claim 56, wherein the metal layer is one of a nickel layer and a nickel alloy layer.

60. (New) The method of claim 38, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.

61. (New) The method of claim 39, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

62. (New) The method of claim 39, wherein forming the insulated gate pattern comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

sequentially patterning the sacrificial layer and the silicon layer.

63. (New) The method of claim 62, further comprising doping the silicon layer with impurities to control a threshold voltage prior to formation of the sacrificial layer.

64. (New) The method of claim 63, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form a buffer layer pattern before patterning the silicon layer, and the buffer layer pattern is removed along with the sacrificial layer pattern to expose the silicon pattern.

65. (New) The method of claim 63, wherein the impurities to control the threshold voltage are N-type.

66. (New) The method of claim 63, wherein the impurities to control the threshold voltage are P-type.

67. (New) The method of claim 39, further comprising doping the silicon layer on top of the semiconductor substrate with impurities to control a threshold voltage.

68. (New) The method of claim 39, further comprising injecting impurity ions into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD and a halo prior to formation of the spacers.

69. (New) The method of claim 68, further comprising forming offset spacers covering the sidewalls of the gate pattern prior to formation of the LDD and the halo.

70. (New) The method of claim 39, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern.

71. (New) The method of claim 70, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

72. (New) The method of claim 39, wherein converting the exposed silicon pattern into a gate silicide layer and concurrently forming source/drain silicide layers, comprises

forming a metal layer on the semiconductor substrate having the exposed silicon pattern; annealing the metal layer until the exposed silicon pattern is silicided; and

removing the unreacted portion of the metal layer remaining on the spacers.

73. (New) The method of claim 72, wherein the metal layer comprises at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

74. (New) The method of claim 72, wherein the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti.

75. (New) The method of claim 72, wherein the metal layer is one of a nickel layer and a nickel alloy layer.

76. (New) The method of claim 40, further comprising injecting impurity ions into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers.

77. (New) The method of claim 43, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

78. (New) The method of claim 43, further comprising forming a buffer layer on top of the silicon layer, wherein the buffer layer is etched to form buffer layer patterns before patterning the silicon layer, and the buffer layer patterns are removed along with the sacrificial layer patterns in order to expose the silicon patterns.

79. (New) The method of claim 43, further comprising injecting impurity ions into the

NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers.

80. (New) The method of claim 43, further comprising forming offset spacers covering the sidewalls of the gate patterns prior to formation of the LDDs and the halos.

81. (New) The method of claim 43, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer patterns.

82. (New) The method of claim 81, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

83. (New) The method of claim 43, wherein converting the exposed silicon patterns into gate silicide layers and concurrently selectively forming source/drain silicide layers, comprises:

i) forming a metal layer on the semiconductor substrate having the exposed silicon patterns;

ii) annealing the metal layer until the exposed silicon patterns are silicided; and

iii) removing the unreacted portion of the metal layer remaining on the spacers.

84. (New) The method of claim 83, wherein the metal layer is at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

85. (New) The method of claim 83, wherein the metal layer comprises an alloy comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

86. (New) The method of claim 83, wherein the metal layer is a nickel layer or a nickel alloy layer.

87. (New) The method of claim 43, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.

88. (New) The method of claim 44, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

89. (New) The method of claim 44, wherein the step of forming the gate patterns comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

patterning the sacrificial layer and the silicon layer.

90. (New) The method of claim 89, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region with impurities to control threshold voltages prior to formation of the sacrificial layer.

91. (New) The method of claim 89, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form buffer layer patterns before patterning the silicon layer, and the buffer layer patterns are removed along with the sacrificial layer patterns in order to expose the silicon patterns.

92. (New) The method of claim 90, wherein the impurities for doping the silicon layer

on the upper portion of the NMOS transistor region and the PMOS transistor region to control the threshold voltages are N-type and P-type, respectively.

93. (New) The method of claim 89, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region on the semiconductor substrate having the sacrificial layer with impurities to control threshold voltages.

94. (New) The method of claim 44, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer patterns.

95. (New) The method of claim 94, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

96. (New) The method of claim 44, wherein converting the exposed silicon patterns into gate silicide layers and concurrently selectively forming source/drain silicide layers, comprises:

i) forming a metal layer on the semiconductor substrate having the exposed silicon patterns;

ii) annealing the metal layer until the exposed silicon patterns are silicided; and

iii) removing the unreacted portion of the metal layer remaining on the spacers.

97. (New) The method of claim 96, wherein the metal layer is at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

98. (New) The method of claim 96, wherein the metal layer comprises an alloy comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

99. (New) The method of claim 96, wherein the metal layer is a nickel layer or a nickel alloy layer.

100. (New) The method of claim 44, further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern.

101. (New) The method of claim 45, wherein the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate.

102. (New) The method of claim 45, wherein the step of forming the gate patterns comprises:

sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate;

forming a sacrificial layer on the semiconductor substrate having the silicon layer; and

patterning the sacrificial layer and the silicon layer.

103. (New) The method of claim 102, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region with impurities to control threshold voltages prior to formation of the sacrificial layer.

104. (New) The method of claim 103, further comprising forming a buffer layer on top of the silicon layer before doping the silicon layer, wherein the buffer layer is etched to form buffer layer patterns before patterning the silicon layer, and the buffer layer patterns are removed along with the sacrificial layer patterns in order to expose the silicon patterns.

105. (New) The method of claim 103, wherein the impurities for doping the silicon

layer on the upper portion of the NMOS transistor region and the PMOS transistor region to control the threshold voltages are N-type and P-type, respectively.

106. (New) The method of claim 102, further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region on the semiconductor substrate having the sacrificial layer with impurities to control threshold voltages.

107. (New) The method of claim 45, further comprising injecting impurity ions into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers.

108. (New) The method of claim 45, further comprising forming offset spacers covering the sidewalls of the gate patterns prior to formation of the LDDs and the halos.

109. (New) The method of claim 45, wherein the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer patterns.

110. (New) The method of claim 109, wherein the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer.

111. (New) The method of claim 45, wherein converting the exposed silicon patterns into gate silicide layers and concurrently selectively forming source/drain silicide layers, comprises:

i) forming a metal layer on the semiconductor substrate having the exposed silicon patterns;

ii) annealing the metal layer until the exposed silicon patterns are silicided; and

iii) removing the unreacted portion of the metal layer remaining on the spacers.

112. (New) The method of claim 111, wherein the metal layer is at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

113. (New) The method of claim 111, wherein the metal layer comprises an alloy comprising a metal selected from the group consisting of Ni, Co, W, and Ti.

114. (New) The method of claim 111, wherein the metal layer is a nickel layer or a nickel alloy layer.

115. (New) The method of claim 46, further comprising forming offset spacers covering the sidewalls of the gate prior to formation of the LDD and the halo.